Exam

Name_____

TRUE/FALSE. Write 'T' if the statement is true and 'F' if the statement is false.

1) The values of an analog signal flow smoothly from one to the next. 1) _____
Answer: True False

2) A sinusoidal waveform is an analog signal. 2) _____
Answer: True False

3) Digital data can be processed and transmitted more efficiently and reliably than analog information. 3) _____
Answer: True False

4) The field that comprises both mechanical and electronic components is known as electro-mechanics. 4) _____
Answer: True False

5) The decimal number system uses nine different symbols. 5) _____
Answer: True False

6) The binary number system uses just two symbols. 6) _____
Answer: True False

7) A waveform that repeats itself at fixed intervals is called a *periodic* waveform. 7) _____
Answer: True False

8) Digital systems respond to voltage levels that change abruptly between two levels (high and low). 8) _____
Answer: True False

9) The amplitude of a digital waveform is the difference in voltage between the LOW and HIGH levels. 9) _____
Answer: True False

10) The clock signal synchronizes the other waveforms in a circuit. 10) _____
Answer: True False

11) Clock signals carry pieces of information such as letters and numbers. 11) _____
Answer: True False

12) Serial data is sent along a single conductor, one bit at a time. 12) _____
Answer: True False

13) Parallel data is sent along a single conductor, one bit at a time. 13) _____
Answer: True False

14) When the inputs to a 2-input AND gate are both HIGH, the output is HIGH. 14) _____

Answer: True False

15) When either input to a 2-input AND gate is LOW, the output is LOW. 15) _____

Answer: True False

16) When either input to a 2-input OR gate is HIGH, the output is HIGH. 16) _____

Answer: True False

17) When both inputs to a 2-input OR gate are both LOW, the output is LOW. 17) _____

Answer: True False

18) When the input to a logic inverter is HIGH, the output is LOW. 18) _____

Answer: True False

19) Encoders and decoders perform opposite conversions. 19) _____

Answer: True False

20) A multiplexer converts parallel data to serial data. 20) _____

Answer: True False

21) A demultiplexer is sometimes called a *mux*. 21) _____

Answer: True False

22) A flip-flop is a 1-bit storage device. 22) _____

Answer: True False

23) The DIP package style has two parallel rows of through-hole pins. 23) _____

Answer: True False

24) The PLCC package has J-type leads on all four edges. 24) _____

Answer: True False

25) The flat-pack (FP) IC package style is a surface-mount device. 25) _____

Answer: True False

26) The FPGA is a fixed-function device. 26) _____

Answer: True False

MULTIPLE CHOICE. Choose the one alternative that best completes the statement or answers the question.

27) A circuit that converts an analog waveform to a digital signal is commonly called a(n) _____. 27) _____

A) DAC B) PLD C) CAD D) ADC

Answer: D

28) A circuit that converts an digital signal to an analog waveform is commonly called a(n) _____. 28) _____

A) PLD B) CAD C) DAC D) ADC

Answer: C

29) Of the circuits listed, the one that is most likely to be found in a CD player is a(n) _____. 29) _____

A) programmable logic device B) SPLD

C) analog-to-digital converter D) digital-to-analog converter

Answer: D

30) On a negative-going pulse, _____. 30) _____

A) HIGH = 1 and LOW = 0 B) HIGH = 0 and LOW = 1

C) LOW = -1 and HIGH = 1 D) HIGH = 0 and LOW = -1

Answer: B

31) On a digital waveform, the transition time from a LOW level to a HIGH level is called _____. 31) _____

A) period B) fall time C) rise time D) pulse width

Answer: C

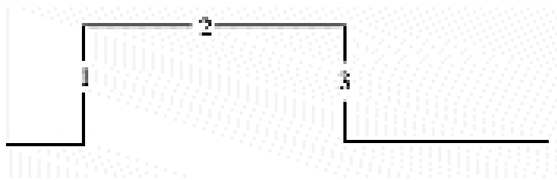


Figure 1-1

32) Which edge in Figure 1-1 is the leading edge? 32) _____

A) 1 B) 2 C) 3 D) Both 1 and 3

Answer: A

33) Which edge in Figure 1-1 is the trailing edge? 33) _____

A) 1 B) 2 C) 3 D) Both 1 and 3

Answer: C

34) The time between transition 1 and transition 3 in Figure 1-1 is the _____. 34) _____

A) pulse width B) period C) amplitude D) frequency

Answer: A

35) On a digital waveform, the transition time from a HIGH level to a LOW level is called _____. 35) _____

A) fall time B) period C) pulse width D) rise time

Answer: A

36) The time from one leading edge on a digital waveform to the next is the waveform _____. 36) _____

A) rise time B) fall time C) period D) pulse width

Answer: C

37) A periodic digital waveform _____. 37) _____

A) has both a HIGH and LOW levels B) repeats itself at a fixed interval

C) has a duty cycle D) all of the above

Answer: D

38) The transition times for an ideal digital pulse are _____. 38) _____

A) infinite

B) measured between 10% to 90% of the amplitude

C) measured between 0 and 90% of the amplitude

D) zero

Answer: D

39) An oscilloscope display indicates that the period of a digital waveform is 40 µs. What is frequency of this waveform? 39) _____

A) 25 kHz

B) 2.5 kHz

C) 40 MHz

D) The frequency cannot be determined using the information provided.

Answer: A

40) What is the duty cycle of a digital waveform with a pulse width of 10 ms a period of 90 ms? 40) _____

A) 90% B) 11.1% C) 10% D) 9%

Answer: B

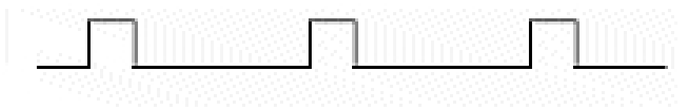
41) On a positive-going pulse, the leading edge is the _____. 41) _____

A) positive-going edge B) negative-going edge

C) falling edge D) HIGH-to-LOW transition

Answer: A

42) The approximate duty cycle for the digital waveform below is _____. 42) _____



A) 80% B) 50% C) 20% D) 30%

Answer: C

43) On a negative-going pulse, the leading edge is the _____. 43) _____

A) LOW-to-HIGH transition B) negative-going edge

C) rising edge D) positive-going edge

Answer: B

44) On a positive-logic pulse, the trailing edge is the _____. 44) _____

A) positive-going edge B) falling edge

C) rising edge D) LOW-to-HIGH transition

Answer: B

45) On a negative-logic pulse, the trailing edge is the _____. 45) _____

A) HIGH-to-LOW transition B) negative-going edge

C) falling edge D) positive-going edge

Answer: D

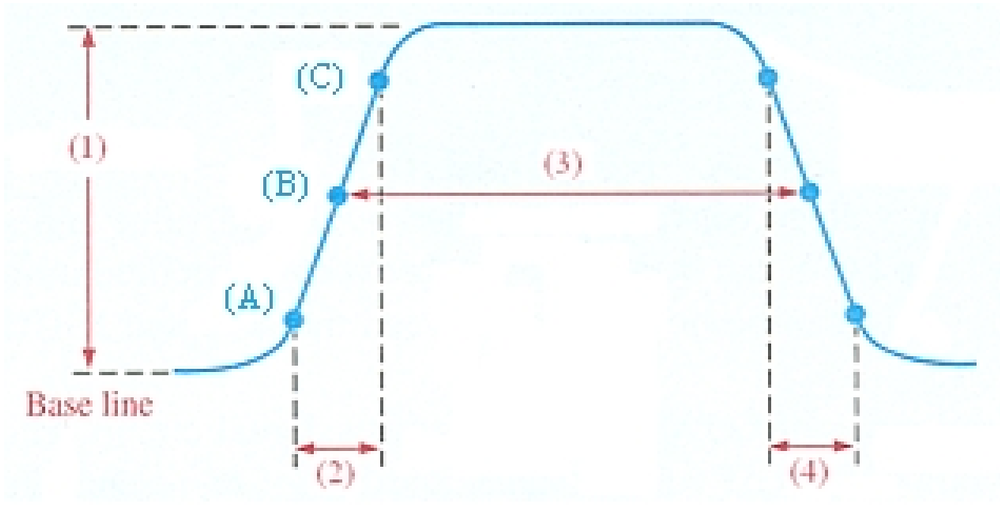


Figure 1-2

46) Item (1) of the nonideal pulse in Figure 1-2 represents the waveform _____. 46) _____

A) transition time B) pulse width C) period D) amplitude

Answer: D

47) Item (2) of the nonideal pulse in Figure 1-2 represents the waveform _____. 47) _____

A) amplitude B) rise time C) fall time D) pulse width

Answer: B

48) Item (3) of the nonideal pulse in Figure 1-2 represents the waveform _____. 48) _____

A) amplitude B) rise time C) fall time D) pulse width

Answer: D

49) Item (4) of the nonideal pulse in Figure 1-2 represents the waveform _____. 49) _____

A) amplitude B) rise time C) fall time D) pulse width

Answer: C

50) When data is set along a single conductor, it is referred to as _____. 50) _____

A) simultaneous data B) serial data

C) parallel data D) none of these

Answer: B

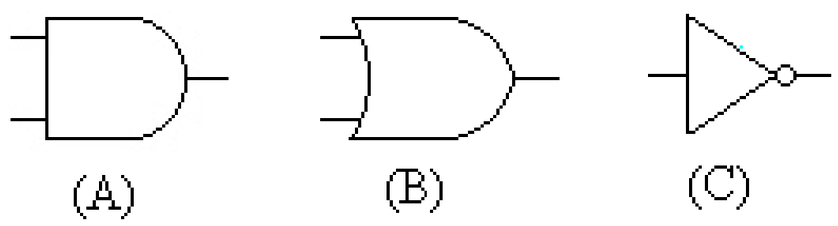


Figure 1-3

51) The symbol in Figure 1-3(A) represents the _____ function. 51) _____

A) AND B) OR C) NOT D) AND/OR

Answer: A

52) The symbol in Figure 1-3(B) represents the _____ function. 52) _____
A) NON B) XOR C) OR D) AND
Answer: C

53) The symbol in Figure 1-3(C) represents the _____ function. 53) _____
A) AND B) OR C) NOT D) XOR
Answer: C

54) The output from an AND gate is HIGH when _____. 54) _____
A) one input is LOW and the remaining inputs are HIGH
B) one input is HIGH and the remaining inputs are LOW
C) all inputs are HIGH
D) all inputs are LOW
Answer: C

55) The output from an AND gate is LOW _____. 55) _____
A) only when all inputs are LOW B) when at least one input is LOW
C) only when all inputs are HIGH D) none of the above
Answer: B

56) The output from an OR gate is HIGH _____. 56) _____
A) only when all inputs are HIGH B) when at least one input is HIGH
C) only when all inputs are LOW D) none of the above
Answer: B

57) The output from an OR gate is LOW _____. 57) _____
A) only when all inputs are LOW B) whenever any input is HIGH
C) only when all inputs are HIGH D) none of the above
Answer: A

58) Which circuit creates an output that indicates whether or not the input values are equal? 58) _____
A) Comparator B) Encoder C) Decoder D) Multiplexer
Answer: A

59) Which circuit converts information into a specific coded form? 59) _____
A) Comparator B) Encoder C) Decoder D) Multiplexer
Answer: B

60) Which circuit converts coded information into a noncoded form? 60) _____
A) Comparator B) Encoder C) Decoder D) Multiplexer
Answer: C

61) Which circuit converts data from serial form to parallel form? 61) _____
A) Demultiplexer B) Encoder C) Comparator D) Multiplexer
Answer: A

62) Which one of the following is not a binary arithmetic function? 62) _____

A) Multiplexing B) Subtraction C) Division D) Addition

Answer: A

63) Two kinds of data selectors are _____ and _____. 63) _____

A) encoders, decoders B) comparators, registers

C) multiplexers, demultiplexers D) adders, subtractors

Answer: C

64) Which one of the circuits listed is made up of flip-flops? 64) _____

A) A converter B) A comparator C) A multiplexer D) A register

Answer: D

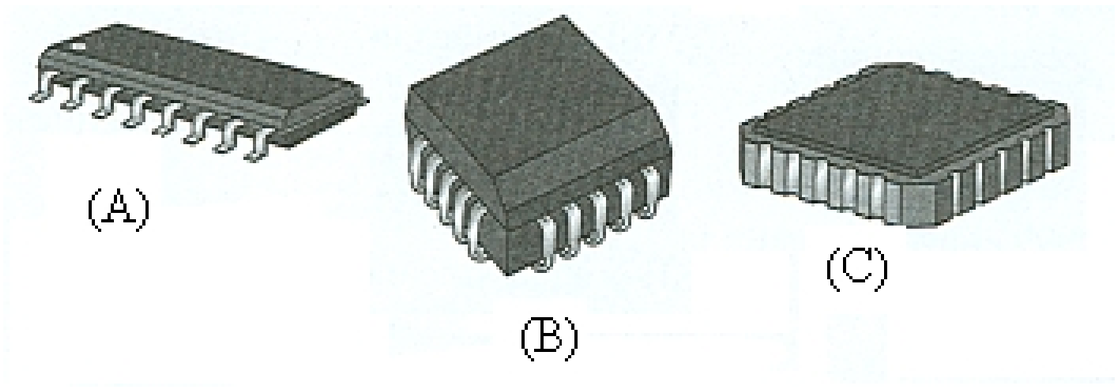


Figure 1-4

65) The package style in Figure 1-4(A) is a(n) _____. 65) _____

A) SOIC B) PLCC C) LCCC D) FP

Answer: A

66) The package style in Figure 1-4(B) is a(n) _____. 66) _____

A) SOIC B) PLCC C) LCCC D) FP

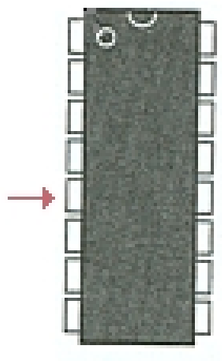
Answer: B

67) The package style in Figure 1-4(C) is a(n) _____. 67) _____

A) SOIC B) PLCC C) LCCC D) FP

Answer: C

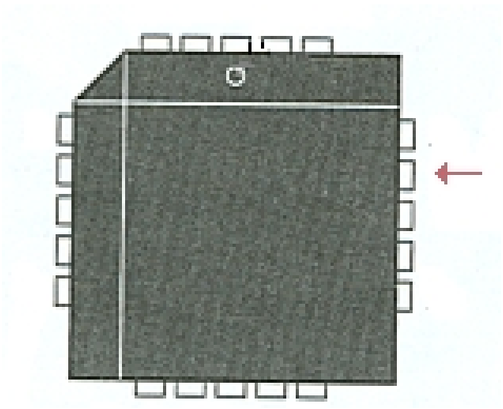
68) The arrow in the figure below points to pin number _____. 68) _____



A) 4 B) 13 C) 12 D) 5

Answer: D

69) The arrow in the figure below points to pin _____. 69) _____



A) 4 B) 17 C) 16 D) 5

Answer: B

70) Which IC package style has no leads? 70) _____

A) PLCC B) SOIC

C) LCCC D) All must have leads.

Answer: C

71) Which one of the following is not a surface-mount IC package? 71) _____

A) FP B) SOIC C) PLCC D) DIP

Answer: D

72) The first step in the PLD programming process is _____. 72) _____

A) design entry B) compilation C) synthesis D) download

Answer: A

73) The final step in the PLD programming process is _____. 73) _____

A) design entry B) compilation C) synthesis D) download

Answer: D

74) The netlist is generated during the _____ phase of the PLD programming process. 74) _____

A) design entry B) compilation C) synthesis D) download

Answer: C

75) Which of the following is an example of a mechatronics system? 75) _____

A) An industrial robot B) A surgical laser

C) A laptop computer D) None of the above

Answer: A